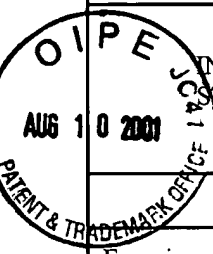






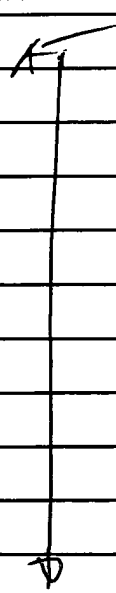
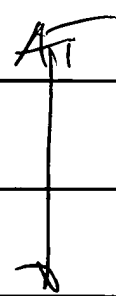


Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 0325.00292		SERIAL NO. 09/475,879		
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT: Timothy M. Lacey et al.				
		FILING DATE December 30, 1999		GROUP 2819		
U.S. PATENT DOCUMENTS						
Examiner Initial	Document No.	Date	Name	Class	Sub- Class	Filing Date
	4 8 7 8 2 0 0	10/31/1989	Asghar et al.	365	189.02	
	5 1 3 6 1 8 8	8/4/1992	Ha et al.	307	465	
	5 2 8 0 2 0 2	1/18/1994	Chan et al.	307	465	
	5 3 8 4 7 4 5	1/24/1995	Konishi et al.	365	230.03	
	5 4 2 2 8 2 3	6/6/1995	Agrawal et al.	364	489	
	5 4 5 1 8 8 7	9/19/1995	El_Avat et al.	326	39	
	5 4 5 5 5 2 5	10/3/1995	Ho et al.	326	41	
	5 5 2 1 5 2 9	5/28/1996	Agrawal et al.	326	41	
	5 5 3 7 0 5 7	7/16/1996	Leong et al.	326	41	
	5 7 8 1 0 3 0	7/14/1998	Agrawal et al.	326	39	
	5 7 9 9 1 7 6	8/25/1998	Kapusta et al.	395	556	
FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub- Class	Transl. Yes No
	"HYBRID PRODUCT TERM AND LUT BASED ARCHITECTURES USING EMBEDDED MEMORY BLOCKS", By Frank Heile and Andrew Leaver, pp. 13-16.					
	"AN INNOVATIVE, SEGMENTED HIGH PERFORMANCE FPGA FAMILY WITH VARIABLE-GRAIN-ARCHITECTURE AND WIDE-GATING FUNCTIONS", By Om Agrawal et al., pp. 17-26.					
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	"XC4000E AND XC4000X SERIES FIELD PROGRAMMABLE GATE ARRAYS", XILINX, May 14, 1996 (Version 1.6), pp. 6-5 to 6-72.					
	"XC4000XLA/XV FIELD PROGRAMMABLE GATE ARRAYS", XILINX, October 18, 1999, pp. 6-157 to 6-170.					
	"VIRTEX™ 2.5V FIELD PROGRAMMABLE GATE ARRAYS", XILINX, April 2, 2001, pp. 1-20.					
Examiner <u>10/5/01</u>			Date Considered 			
Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						

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U.S. PATENT DOCUMENTS						
Examiner Initial	Document No.	Date	Name	Class	Sub- Class	Filing Date
	5 8 1 1 9 8 7	9/22/1998	Ashmore, Jr. et al.	326	39	
	5 8 1 8 2 5 4	10/6/1998	Agrawal et al.	326	39	
	5 8 4 8 2 8 5	12/8/1998	Kapusta et al.	395	800.01	
	5 9 6 6 0 2 7	10/12/1999	Kapusta et al.	326	39	
	6 0 4 9 2 2 3	4/11/2000	Lytle et al.	326	40	
	6 0 5 8 4 5 2	5/2/2000	Rangasayee et al.	711	108	
	6 1 3 4 1 8 1	10/17/2000	Landry	365	233	
	6 1 3 7 3 0 8	10/24/2000	Nayak	326	39	
	6 1 9 1 9 9 8	2/20/2001	Reddy et al.	365	230.05	
	6 2 0 1 4 0 7	3/13/2001	Kapusta et al.	326	39	
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	Document No.	Date	Country	Class	Sub- Class	Transl. Yes No
OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)						
	"COOLRUNNER® XPLA3 CPLD", XILINX, April 11, 2001, pp. 1-10.					
	"SPARTAN AND SPARTAN-XL FAMILIES FIELD PROGRAMMABLE GATE ARRAYS", XILINX, March 2, 2000, pp. 4-1 to 4-66.					
	"XC9500XV FAMILY HIGH-PERFORMANCE CPLD", XILINX, January 15, 2001, pp. 1-18.					
	"INTEGRATED PRODUCT-TERM LOGIC IN APEX 20K DEVICES", ALTERA, April 1999, ver. 1.0, pp. 1-12.					
	"APEX II PROGRAMMABLE LOGIC DEVICE FAMILY", ALTERA, May 2001, ver. 1.1, pp. 1-96.					
	"FLEX 8000 PROGRAMMABLE LOGIC DEVICE FAMILY", ALTERA, June 1999, ver. 10.01, pp. 349-410.					
Examiner			Date Considered <u>10/5/01</u>			
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